Hyunsung Jeong

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Education

Ulsan National Institute of Science and Technology (UNIST) Mar. 2021 – Feb. 2027
Ulsan, Republic of Korea
Bachelor of Engineering in Electrical and Electronic Engineering
Overall GPA: 4.22 / 4.30 **Major GPA: 4.30 / 4.30**

Publications

[C1] **Hyunsung Jeong***, Kyounghun Kang*, Jongeun Lee, and Wanyeong Jung. "B-Flex: Exploration of Broader Flip-Flop Design Space Based on FSM Exhaustive Search". ***In Proc. Design Automation Conf. (DAC)***, 2026. (*Equal contribution)

[C2] **Hyunsung Jeong**, Sanhtet Aung, and Jongeun Lee. "SoDA: Schema-Driven Co-Exploration of Hardware and Mapping for DNN Accelerators". Under review.

Research Interests

My research focuses on abstraction-driven hardware design methodologies, including logic-level validation, design space exploration, and architecture–mapping co-design for DNN accelerators. I am particularly interested in building practical flows that connect high-level design abstractions to synthesizable and verifiable hardware implementations.

Research Experience

Research Assistant, ICCL Lab, UNIST Aug. 2025 – Present
Advisor: Prof. Jongeun Lee.

Project: Logic-Aware Validation and Search Methodology for Stateful Hardware Design [C1]

Aug. 2025 – Nov. 2025

Co-advised by Prof. Jongeun Lee and Prof. Wanyeong Jung.

- **Motivation.** Addressed the limited scalability of prior flip-flop exploration methods, which were constrained by incomplete validation and inefficient brute-force FSM search.
- Identified incompleteness in prior FSM-based flip-flop validation, showing that test-vector-based checking can miss invalid state-transition behavior.
- Formalized flip-flop correctness as an inductive invariant between circuit-level asynchronous FSMs and logical reference behavior.
- Proposed and implemented a validation-guided search algorithm that prunes invalid candidates early while preserving the complete valid design space.
- **Impact.** Enabled exhaustive exploration of broader flip-flop mechanisms, discovering hundreds of millions of valid FSMs and synthesized designs that outperform conventional flip-flops.

Project: Dataflow-Centric Co-Design Framework for DNN Accelerators [C2]

Dec. 2025 – Apr. 2026

- **Motivation.** Addressed the scalability challenge of DNN accelerator design space exploration, where hardware and mapping decisions are tightly coupled in a large, unstructured joint space.
- Formalized dataflow characteristics as transfer counts and proposed a Pareto-preserving pruning strategy to eliminate inferior hardware–mapping candidates.
- Developed a schema-based abstraction that captures operand reuse across execution contexts and structures the joint hardware–mapping design space.
- Implemented a co-exploration framework and evaluated Pareto-competitive accelerator designs for CNN and Transformer workloads using the Timeloop simulator.
- **Impact.** Demonstrated that schema-driven exploration can identify high-quality accelerator designs with substantially fewer evaluations and lower EDP than strong baseline methods.

Project: From DSE Abstractions to Synthesizable Accelerator Designs
May 2026 – Present

- **Motivation.** Addressing the gap between high-level DSE abstractions and concrete RTL realization in accelerator design.
- Implementing a Chisel-based, layer-wise accelerator generation flow that translates architecture–mapping descriptions into synthesizable hardware structures.
- Exploring hardware-aware compilation methods that translate mapping decisions into execution schedules, data movement patterns, and hardware control logic.

Coursework & Projects

Selected Coursework: Advanced Computer Architecture, Tensor Processor Design, Computer Architecture, VLSI Design, Digital Logic Design and Lab, Electronic Circuits I/II and Lab, Semiconductor Engineering, Automatic Control.

FPGA-Based Streaming Accelerator for MNIST Inference Spring 2026
Course project for Tensor Processor Design; Instructor: Prof. Jongeun Lee.

- Implemented a streaming CNN/BNN inference accelerator on a Xilinx PYNQ-Z2, processing the full 70K-image MNIST dataset in 0.13 seconds.
- Designed a dual-core accelerator architecture with independent data routes to exploit data-level parallelism and reduce end-to-end inference latency.
- Optimized the accelerator using bit-packed activations, XOR-popcount computation, line buffers, DATAFLOW pipelining, and HLS loop directives.

Topology-Aware Optimization of MoE Expert Placement Spring 2026
Course project for Advanced Computer Architecture; Instructor: Prof. Ranggi Hwang.

- Formulated MoE expert placement and dispatch as a topology-aware optimization problem for distributed multi-GPU inference.
- Built a differentiable latency model that captures all-to-all communication, expert load imbalance, GPU capacity, and replica dispatch decisions.
- Applied gradient-based optimization to jointly tune expert placement and replica-dispatch decisions, reducing end-to-end latency compared with capacity-saturated round-robin and random-search baselines.

Honors

Unhae Scholarship Feb. 2026
Merit-based scholarship, KRW 8,000,000, approximately USD 5,500.

Dean's List Award, College of Engineering Feb. 2023, Aug. 2025
Recognized for exceptional academic achievement in the Department.

New Student Division Award for Academic Excellence Feb. 2022
Awarded to one of the top three first-year students across UNIST.

UNIST Full-Tuition Scholarship Mar. 2021 – Feb. 2027
Received university-funded tuition support for all eight undergraduate semesters.

Skills

Languages: C++, Python, Verilog HDL, Chisel/Scala (basic)
Hardware: Xilinx Vitis HLS, Xilinx Vivado Design Suite
Parallel Programming: CUDA, OpenMP